

Complete Boolean Algebra for Memristive and Spintronic Asymmetric Basis Logic Functions

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Abstract—The increasing advancement of emerging device technologies that provide alternative basis logic sets necessitates the exploration of innovative logic design automation methodologies. Specifically, emerging computing architectures based on the memristor and the bilayer avalanche spin-diode offer non-commutative or ‘asymmetric’ operations, namely the inverted-input AND (IAND) and implication as basis logic gates. Existing logic design techniques inadequately leverage the unique characteristics of asymmetric logic functions resulting in insufficiently optimized logic circuits. This paper presents a complete Boolean algebraic framework specifically tailored to asymmetric logic functions, introducing fundamental identities, theorems and canonical normal forms that lay the groundwork for efficient synthesis and minimization of such logic circuits without relying on conventional Boolean algebra. Further, this paper establishes a logical relationship between implication and IAND operations. A previously proposed modified Karnaugh map method based on a subset of the presented algebraic principles demonstrated a 28% reduction in computational steps for an algorithmically designed memristive full adder; the presently-proposed algebraic framework lays the foundation for much greater future improvements.

Index Terms—Asymmetric logic, beyond-CMOS computing, Boolean algebra, emerging technologies, memristors, spintronics

I. INTRODUCTION

Over the last five decades, progress in fabrication technology has enabled the continued downscaling of CMOS-based devices that has contributed to consistent improvements in the performance of integrated circuits (ICs) in accordance with Moore’s Law [1], [2]. However, achieving further scaling becomes exceedingly challenging as the transistor device size approaches a few atomic layers, triggering the onset of quantum effects [3]–[5]. This may result in heightened leakage current caused by quantum tunneling, consequently raising the standby power dissipation [6], [7]. Fortunately, in the pursuit of finding alternative technologies, several promising proposals have been put forth, including magnetic tunnel junction logic [8], [9], domain wall logic [8], [10]–[13], all-carbon spin logic [14], reversible skyrmion logic [15], spin-FETs [16]–[19] that use magnets and electron spin as state variables instead of charge currents, and other spin based logic systems [20]–[22].

As newer devices emerge, it is imperative that progress in logic design matches the pace of device research through

refinement of existing logic synthesis and minimization techniques that suit these novel device technologies. Specific device challenges and opportunities include the bilayer avalanche spin-diode device [21] can be used to perform logical OR or an inverted-input AND (IAND) function, while the memristor-based stateful logic [23], [24] efficiently performs the implication (IMPLY) and NAND boolean functions. Each of the IMPLY and IAND boolean logic operations are logically ‘asymmetric’, meaning that they are non-commutative in nature. In many previous studies, logic minimization is conducted using a basis set of traditional logic functions, whereby each foundational logic gate is mapped to an efficient memristor implementation. For instance, [25] minimizes a function into OR and inverter gates, while [26] utilizes NOT, NAND and OR gates for minimization. Most notably, [27] minimizes a substantial function into NAND, OR, and parity gates, subsequently implementing them with memristors. Further, [28] employs majority gates to achieve optimized circuits, and while [29] focuses on minimizing the number of memristors, it does not present a way to reduce the number of computational steps. Binary decision diagrams [30] and CMOS buffer circuits [31] have also been applied, as well as an interpretation of memristors as threshold logic elements [32]. Since all of these methodologies involve optimizing logic circuits using conventional symmetric Boolean algebraic principles, the resulting circuits fail to fully capitalize on the asymmetric basis logic operations offered by memristors.

Previously, we have introduced a modified Karnaugh map method to minimize asymmetric logic circuits without the need to deploy conventional Boolean algebra [33]. A full adder circuit designed using the proposed minimization algorithm achieved a 28 percent reduction in the number of computational steps when compared to the best [24] manually-optimized full adder. While the foundational Boolean algebraic principles underlying the modified Karnaugh map method were briefly outlined, this article presents a complete set of Boolean algebraic identities and theorems tailored to asymmetric logic functions. For completeness, this includes the principles that have already been laid out in our previous work. Section II details the background for the device technologies, asymmetric logic functions and the previously proposed Karnaugh map method for asymmetric logic, while Section III presents the algebraic theorems and identities with necessary proofs. Section IV provides concluding remarks.

II. BACKGROUND

Both the bilayer avalanche spin-diode and memristor offer a distinct set of basis logic operations. A single bilayer

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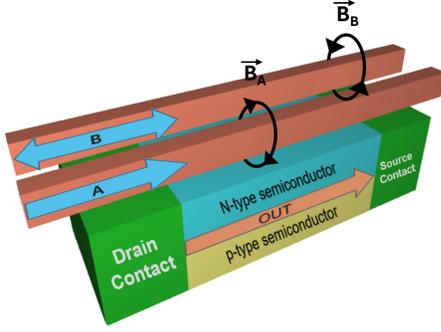


Fig. 1. The bilayer avalanche spin-diode. The flow of currents in control wires A and B induces a magnetic field over the semiconductor p-n junction, leading to the modulation of the output current.

avalanche spin-diode unit can perform both IAND and OR functions, while it takes two and three non-volatile memristors to perform an implication and NAND function, respectively. To efficiently leverage these basis logic functions in large-scale systems, it is crucial to acknowledge the logically asymmetric characteristics of the IAND and implication functions. Utilizing conventional logic design techniques to minimize such asymmetric logic functions yields a sub-optimal circuit, as the minimization process is not directly applied to the IMPLY-NAND and IAND-OR logic sets. Therefore, the development of a bespoke algebraic framework becomes imperative to fully harness the potential of such circuits.

A. Bilayer Avalanche Spin-Diode Logic

A bilayer avalanche spin-diode is a two-terminal spintronic device and possesses a negative magnetoresistance that allows an applied magnetic field to alter the resistance. The current passing through the spin-diode is modulated by the current on two control wires A and B (refer to Fig. 1). The voltage across the diode is kept constant, enabling the two input currents to generate magnetic fields that affect the output current of the spin-diode. The resistance state of the spin-diode is dictated by the magnitude and alignment of the magnetic fields relative to a threshold level.

In this system, a ‘1’ is represented by a large current flow, while a ‘0’ is represented by a small current. The device can perform a Boolean OR and an inverted-input AND (IAND) function depending on the relative direction of the control currents. These two functionalities arise from the magnetic fields generated by currents aligned in either the same or opposite directions, which can either reinforce or counteract each other, respectively (see Fig. 2 and Table I). In contrast to memristors, spin-diodes exhibit volatility, reverting to their zero-magnetic field state promptly upon the cessation of applied input currents.

B. Stateful Memristor Logic

Memristors, or ‘memory resistors’ are two-terminal, non-linear electrical components whose resistance changes based on the amount of charge that has previously flown through them [34], [35]. First conceptualized by Leon Chua [34] in

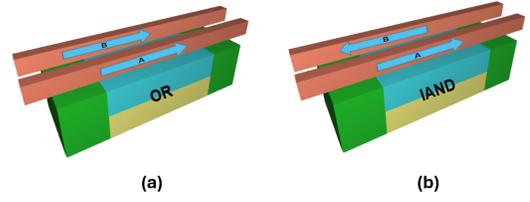


Fig. 2. Bilayer avalanche spin-diode device performs a (a) Boolean OR if the input currents A and B flow in the same direction, and an (b) IAND function if A and B have opposite directions.

TABLE I
TRUTH TABLE FOR IMPLICATION AND IAND LOGIC.

Input A	Input B	IMPLY	IAND
0	0	1	0
0	1	1	0
1	0	0	1
1	1	1	0

1971, the resistance of a memristor is not simply binary (*i.e.*, in a high or low resistance state), but rather exists on a spectrum determined by the history of applied voltages. In an ideal scenario, when the applied voltage exceeds a certain threshold magnitude, it triggers a transition in the memristor’s resistance state to a purely resistive or conductive state. Specifically in Fig. 3:

- Conductive state (1): $V_P - V_N > V_{TH}$ and,
- Resistive state (0): $V_N - V_P > V_{TH}$,

where V_{TH} is the threshold voltage, and V_N and V_P are the voltages at nodes P and N respectively.

Stateful implication, denoted as $OUTPUT = A \rightarrow B$ is achieved by applying V_{COND} to memristor A and V_{SET} to memristor B , maintaining $V_{COND} < V_{TH} < V_{SET}$ and $V_{SET} - V_{COND} < V_{TH}$ [36]. Table I shows the truth table for implication logic. When memristor A is in the resistive state (0), the V_{SET} voltage across memristor B exceeds V_{TH} , prompting memristor B to transition to the conductive state (1) or remain in it. Conversely, if memristor A is in the conductive state (1), the voltage across memristor B is $V_{SET} - V_{COND}$; since this value falls below V_{TH} , no switching occurs. Hence, the IMPLY function can be executed by two memristors in a single step, whereas a NAND function can similarly be executed with three memristors in two steps (see Fig. 5).

Unlike traditional approaches where each cascaded operation requires a distinct set of devices, in stateful memristor logic the memristors are continually reused through a sequential application of V_{SET} and V_{COND} voltages. Table II outlines the sequential steps for implementing the NAND operation between p and q , utilizing s as the output memristor.

C. Asymmetric Basis Logic Functions

Typically, traditional Boolean operations adhere to commutativity, where the order of operands does not affect the outcome. However, asymmetric logic operations deviate from this norm as the result of such operations change when the operands are swapped. Thus, these operations can be characterized as inherently ‘non-commutative’. In this paper,

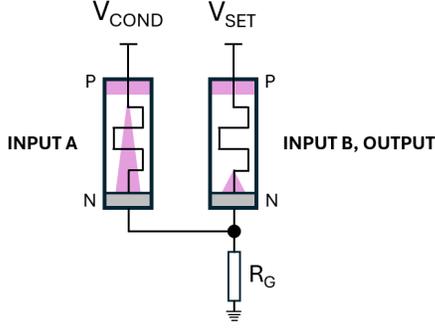


Fig. 3. Schematic diagram illustrating the memristive implication logic, in which the resistance state is modulated by applying voltages to the memristors.

the discussion centers around two such functions: IAND and IMPLY.

The IAND function is an AND function with one input inverted (see Table I). A distinct symbol (Λ) for this operation has been proposed in [33] such that

$$IAND(A, B) = A \wedge \bar{B} = A \Lambda B, \quad (1)$$

whereas, implication operation is defined as

$$IMPLY(A, B) = \bar{A} \vee B = A \rightarrow B. \quad (2)$$

Since in such operations the order of the operands is crucial, the operand to the left (right) side of the IAND (IMPLY) is called the *non-inverted* input, while the remaining operand is called the *inverted* input. Moreover, in scenarios involving more than two operands, only two operands must be computed at a time whilst paying attention to the overall order of operation. The following rules apply to any Boolean expression involving IAND or IMPLY operations:

- IAND: Two operands at a time, from left to right.

$$IAND(A, B, C) = (A \Lambda B) \Lambda C \quad (3)$$

- IMPLY: Two operands at a time, from right to left

$$IMPLY(A, B, C) = A \rightarrow (B \rightarrow C) \quad (4)$$

D. Karnaugh Map Method for Asymmetric Logic Functions

The primary objective behind constructing an entire Boolean logic paradigm based on asymmetric logic sets is to streamline computation and optimization procedures for functions based on such sets, all the while eliminating the necessity to convert them into traditional logic. A comprehensively defined Boolean algebra tailored to asymmetric logic functions serves as the foundation for optimization algorithms, such as the modified Karnaugh map method proposed in [33]. The method is built upon a subset of theorems and identities presented in the subsequent sections of this paper, and enables the efficient design of a memristive full adder algorithmically designed using the proposed technique. The full adder was realized by using the IMPLY-NAND basis logic set, and the sum and carry out equations are denoted as NOI expressions as shown in (5) and (6) respectively.

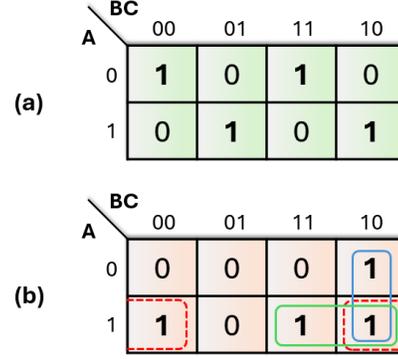


Fig. 4. Karnaugh map representations for the full adder equations: (a) Sum (5). (b) Carry out (6).

$$S_{noi} = \frac{\overline{\{(A \rightarrow (\bar{B} \rightarrow \bar{C})) \wedge (\bar{A} \rightarrow (\bar{B} \rightarrow C))\}}}{\overline{\{(A \rightarrow (B \rightarrow C)) \wedge (\bar{A} \rightarrow (B \rightarrow \bar{C}))\}}} \quad (5)$$

$$C_{noi} = \frac{\overline{\{(\bar{A} \rightarrow (B \rightarrow C)) \wedge (A \rightarrow (\bar{B} \rightarrow C))\}}}{\overline{\{(A \rightarrow (B \rightarrow \bar{C})) \wedge (A \rightarrow (B \rightarrow C))\}}} \quad (6)$$

The carry out expression is then reduced down to (7) by using the suggested K-Map algorithm as shown in Fig. 4.

$$C_{noi} = \overline{(A \rightarrow \bar{C}) \wedge (B \rightarrow \bar{C}) \wedge (A \rightarrow \bar{B})} \quad (7)$$

The resulting full adder realizes a 28% reduction in the number of computational steps as compared to a previously proposed manual optimization approach [24]. Moreover, this enhancement is even greater when applied to larger systems, such as multi-bit adders [33].

III. BOOLEAN ALGEBRA FOR ASYMMETRIC LOGIC FUNCTIONS

The development of a Boolean algebra tailored specifically to asymmetric logic functions is necessary to enhance the efficiency of circuits employing devices that perform such functions inherently. This section provides the algebraic laws that can directly be applied to IAND and IMPLY functions without the need to represent them as conventional logic operations. Furthermore, canonical normal forms are presented to help standardize complex logical expressions involving these functions. Finally, a theoretical relationship between IAND and IMPLY functions is established. The laws governing IAND functions are accompanied by proofs where necessary, and while not explicitly proven for IMPLY functions, they can be demonstrated using a similar approach.

A. Core Algebraic Identities

The fundamental properties of a logic operation are defined by a set of core identities that are essential for simplifying Boolean expressions and ultimately for effective minimization of logic circuits. In this section, we present the essential algebraic identities for IAND and IMPLY functions.

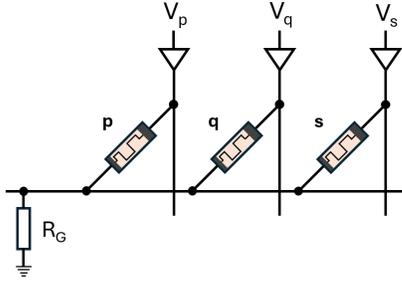


Fig. 5. Standard NAND gate realization using stateful memristive implication.

TABLE II
COMPUTATIONAL STEPS FOR NAND LOGIC REALIZED VIA STATEFUL
MEMRISTIVE IMPLICATION.

Step	Operation	V_{COND} applied to	V_{SET} applied to	V_{RESET} applied to	Output Memristor	State of s
0	RESET	-	-	s	-	$s = 0$
1	$p \rightarrow s$	p	s	-	s	\bar{p}
2	$q \rightarrow s$	q	s	-	s	$\overline{p \wedge q}$

1) *Interaction with High (1) and Low (0) Logic:* These properties define how Boolean functions are altered when operated with IAND and IMPLY operators against a 0 or a 1.

Identity 1 (Annulment Law):

$$(a) \text{ IAND : } A \wedge 1 = 0 \wedge \bar{A} = 0 \quad (8)$$

$$(b) \text{ IMPLY : } A \rightarrow 1 = 1 \quad (9)$$

Proof. Using AND representation for IAND,
 $A \wedge 1 = A \wedge \bar{1} = A \wedge 0 = 0$ (10)

$$\text{and, } 0 \wedge A = 0 \wedge \bar{A} = 0 \quad (11)$$

proving the identity. *Q.E.D.*

Identity 2 (Inversion Law):

$$(a) \text{ IAND : } 1 \wedge A = \bar{A} \quad (12)$$

$$(b) \text{ IMPLY : } A \rightarrow 0 = \bar{A} \quad (13)$$

Proof. Representing the IAND operation in terms of AND,

$$1 \wedge A = 1 \wedge \bar{A} = \bar{A} \quad (14)$$

which proves the identity. *Q.E.D.*

Identity 3 (Identity Law):

$$(a) \text{ IAND : } A \wedge 0 = A \quad (15)$$

$$(b) \text{ IMPLY : } 1 \rightarrow A = A \quad (16)$$

Proof. Representing the IAND operation in terms of AND,

$$A \wedge 0 = A \wedge \bar{0} = A \wedge 1 = A \quad (17)$$

which proves the identity. *Q.E.D.*

2) *Idempotency:* Idempotency is a characteristic that allows operation of a variable with itself without altering its value. Due to the inherent nature of asymmetric functions, true idempotency is unachievable. However, the property can be theorized for the following cases of single-input operations, even though the value of the variable is not preserved. The properties are classified according to their behaviors.

Identity 4 (Null Idempotency):

$$(a) \text{ IAND : } A \wedge A = 0 \quad (18)$$

$$(b) \text{ IMPLY : } A \rightarrow A = 1 \quad (19)$$

Proof. Representing the IAND operation in terms of AND,

$$A \wedge A = A \wedge \bar{A} = 0 \quad (20)$$

which proves the identity. *Q.E.D.*

Identity 5 (Inverse Idempotency - I):

$$(a) \text{ IAND : } A \wedge \bar{A} = A \quad (21)$$

$$(b) \text{ IMPLY : } A \rightarrow \bar{A} = \bar{A} \quad (22)$$

Proof. Representing the IAND operation in terms of AND,

$$A \wedge \bar{A} = A \wedge A = A \quad (23)$$

substantiating the identity. *Q.E.D.*

Identity 6 (Inverse-Idempotency - II):

$$(a) \text{ IAND : } \bar{A} \wedge A = \bar{A} \quad (24)$$

$$(b) \text{ IMPLY : } \bar{A} \rightarrow A = A \quad (25)$$

Proof. Representing the IAND operation in terms of AND,

$$\bar{A} \wedge A = \bar{A} \wedge \bar{A} = \bar{A} \quad (26)$$

proving the identity. *Q.E.D.*

B. Boolean Algebraic Laws

The section elucidates the conventional principles of Boolean Algebra as they apply in the context of asymmetric logic functions. It is noteworthy to mention that certain laws in this exposition may diverge from their conventional definitions; nevertheless, a discernible analogy is apparent for each.

1) *Commutative Law:* The characterization of a Boolean function as 'asymmetric' inherently denotes its departure from the conventional commutative law, *i.e.*

$$A \wedge B \neq B \wedge A \quad (27)$$

$$\text{and, } A \rightarrow B \neq B \rightarrow A. \quad (28)$$

However, a kind of asymmetric commutation is achievable as demonstrated by the following theorem.

Theorem 1 (Asymmetric Commutation): Considering two operands A and B , commutation is realized through complements of each of the literals as illustrated by (29) and (30)

$$A \wedge B = \bar{B} \wedge \bar{A} \quad (29)$$

$$\text{and, } A \rightarrow B = \overline{B} \rightarrow \overline{A} \quad (30)$$

Proof. Replacing the IAND with AND,

$$A \wedge B = A \wedge \overline{B} = \overline{B} \wedge A. \quad (31)$$

Changing the RHS of (31) back to IAND notation,

$$A \wedge B = \overline{B} \wedge \overline{\overline{A}}, \quad (32)$$

which proves the theorem. *Q.E.D.*

2) *Associativity Laws:* Associativity laws delineate the manner in which three or more Boolean functions are paired while being operated by a Boolean operator. It is crucial to note that, owing to the asymmetric inversion of operands, IAND and IMPLY operations do not adhere to associativity in the conventional sense.

Theorem 2 (Conventional ‘Non-Associativity’):

$$(A \wedge B) \wedge C \neq A \wedge (B \wedge C) \quad (33)$$

The above can be proved as follows. Note that the parentheses are solved two-at-a-time from left to right as suggested earlier.

Proof. Converting the two sides of Theorem 2 to AND notation,

$$(A \wedge B) \wedge C = A \wedge \overline{B} \wedge \overline{C} \quad (34)$$

$$A \wedge (B \wedge C) = A \wedge (B \wedge \overline{C}) = A \wedge (\overline{B} \vee C) \quad (35)$$

Clearly, (34) and (35) are not equivalent. *Q.E.D.*

However, asymmetric functions do conform to two special kinds of associativity laws: Inverting and Non-Inverting. These are explained in detail in the following two theorems.

Theorem 3 (Non-Inverting Associativity): Non-inverting associativity denotes a scenario in which altering the order of specific operands does not necessitate inversion. This circumstance arises when the positions of any two ‘inverted’ operands are interchanged.

$$(A \wedge B) \wedge C = (A \wedge C) \wedge B \quad (36)$$

Proof. Converting the expression to AND notation:

$$(A \wedge B) \wedge C = A \wedge \overline{B} \wedge \overline{C} = A \wedge \overline{C} \wedge \overline{B}. \quad (37)$$

This can be rewritten using IAND notation as follows:

$$A \wedge \overline{C} \wedge \overline{B} = (A \wedge C) \wedge B. \quad (38)$$

The theorem is thus proven. *Q.E.D.*

Theorem 4 (Inverting Associativity): Inverting associativity necessitates the inversion of both the operands that have undergone a change in position. This theorem must be employed when a ‘non-inverted’ input interchanges its place with an ‘inverted’ input. For two literals, the law is directly equivalent to Theorem 1, where the inverted operand B trades its position with operand A relative to the IAND/IMPLY operator. For three literals, however,

$$(A \wedge B) \wedge C = (\overline{B} \wedge \overline{A}) \wedge C = (\overline{C} \wedge B) \wedge \overline{A} = (\overline{C} \wedge \overline{A}) \wedge B \quad (39)$$

$$A \rightarrow (B \rightarrow C) = \overline{C} \rightarrow (B \rightarrow \overline{A}) = A \rightarrow (\overline{C} \rightarrow \overline{B})$$

$$= B \rightarrow (\overline{C} \rightarrow \overline{A}) \quad (40)$$

Note that the resultant expression on the RHS in (39) and (40) continue to follow the order of operation for asymmetric logic as described in section II-C.

Proof. Converting the LHS of (39) to AND notation:

$$(A \wedge B) \wedge C = A \wedge \overline{B} \wedge \overline{C}. \quad (41)$$

Rearranging the inputs on the RHS of the above expression,

$$(A \wedge B) \wedge C = \overline{B} \wedge A \wedge \overline{C} = \overline{C} \wedge \overline{B} \wedge A = \overline{C} \wedge A \wedge \overline{B}, \quad (42)$$

which can be rewritten using IAND notation as

$$(A \wedge B) \wedge C = (\overline{B} \wedge \overline{A}) \wedge C = (\overline{C} \wedge B) \wedge \overline{A} = (\overline{C} \wedge \overline{A}) \wedge B, \quad (43)$$

which is the same as (39). *Q.E.D.*

Discussion: Theorem 3 and Theorem 4 can also be interpreted intuitively as the movement of inverted and non-inverted operands around the IAND/IMPLY operators:

- Logical equivalence continues to be maintained if an ‘inverted’ operand trade places with another ‘inverted’ operand (non-inverting associativity).
- Should a ‘non-inverted’ operand interchange positions with an ‘inverted’ operand within the expression, both of these operands are complemented to preserve logical equivalence (inverting associativity).

3) *Distributive Laws:* This section details the distributive laws that govern the interaction of asymmetric operators with the conventional OR and AND logic. Theorems presented here are numbered rather than named individually, since individual nomenclature would be quite challenging and perhaps, confusing. Additionally, it is noteworthy that while some of these theorems may possess greater utility or relevance than others, the entirety of the conceivable combinations of these operations are presented for completeness. Further, the proofs for each of these theorems is akin to the theorems and identities presented thus far, and is hence skipped for brevity.

Theorem 5 (Distributive Law - I):

$$A \wedge (B \wedge C) = (A \wedge B) \wedge (A \wedge C). \quad (44)$$

$$A \rightarrow (B \wedge C) = (A \rightarrow B) \wedge (A \rightarrow C). \quad (45)$$

Theorem 6 (Distributive Law - II):

$$(A \wedge B) \wedge C = (A \wedge B) \wedge \overline{C} \quad (46)$$

$$(A \rightarrow B) \wedge C = (\overline{A} \wedge C) \vee (B \wedge C) \quad (47)$$

Theorem 7 (Distributive Law - III):

$$(A \vee B) \wedge C = (A \wedge C) \vee (B \wedge C) \quad (48)$$

$$(A \vee B) \rightarrow C = (A \rightarrow C) \wedge (B \rightarrow C) \quad (49)$$

Theorem 8 (Distributive Law - IV):

$$A \wedge (B \vee C) = (A \wedge B) \wedge (A \wedge C) \quad (50)$$

$$A \rightarrow (B \vee C) = (A \rightarrow B) \vee C = A \rightarrow (\overline{B} \rightarrow C) \quad (51)$$

Theorem 9 (Distributive Law - V):

$$A \wedge (B \wedge C) = (A \wedge B) \wedge C = (A \wedge \overline{B}) \wedge C \quad (52)$$

$$A \wedge (B \rightarrow C) = (A \wedge \overline{B}) \vee (A \wedge C) \quad (53)$$

Theorem 10 (Distributive Law - VI):

$$A \vee (B \wedge C) = (A \vee B) \wedge (A \vee \overline{C}) \quad (54)$$

$$A \vee (B \rightarrow C) = \overline{A} \rightarrow (B \rightarrow C) \quad (55)$$

Theorem 11 (Distributive Law - VII):

$$(A \wedge B) \vee C = (A \vee C) \wedge (\overline{B} \vee C) \quad (56)$$

$$(A \wedge B) \rightarrow C = A \rightarrow (B \rightarrow C) \quad (57)$$

4) *De Morgan's Law for Asymmetric Logic*: By now it is evident that traditional Boolean laws do not apply to asymmetric logic operations without requisite modifications. Fortunately, for the De Morgan's rule, there is a notable resemblance between the proposed modified version for IAND/IMPLY logic and the established convention. The De Morgan's law as applied to asymmetric logic operations can be formally stated as,

Theorem 12: (A) The negation of ordered IAND of two literals is equal to the OR of the two literals with the non-inverted term complemented.

(B) The negation of ordered implication of two literals is equal to the NAND of the two literals with the non-inverted term complemented.

For two inputs:

$$(a) \text{ IAND} : \overline{(A \wedge B)} = \overline{A} \vee B \quad (58)$$

$$(b) \text{ IMPLY} : \overline{(A \rightarrow B)} = A \wedge \overline{B} \quad (59)$$

Conversely,

$$(a) \text{ IAND} : \overline{(A \vee B)} = \overline{A} \wedge B \quad (60)$$

$$(b) \text{ IMPLY} : \overline{(A \wedge B)} = A \rightarrow \overline{B} \quad (61)$$

For three inputs:

$$(a) \text{ IAND} : \overline{((A \wedge B) \wedge C)} = \overline{A} \vee B \vee C \quad (62)$$

$$(b) \text{ IMPLY} : \overline{(A \rightarrow (B \rightarrow C))} = A \wedge B \wedge \overline{C} \quad (63)$$

Conversely,

$$(a) \text{ IAND} : \overline{(A \vee B \vee C)} = (\overline{A} \wedge B) \wedge C \quad (64)$$

$$(b) \text{ IMPLY} : \overline{(A \wedge B \wedge C)} = A \rightarrow (B \rightarrow \overline{C}) \quad (65)$$

For memristive circuits, the De-Morgan's rule can be restated in terms of the fundamental IMPLY/NAND logic set as follows. Note that the inverter can easily be realized using a NAND gate with inputs shorted.

$$\overline{(A \rightarrow B)} = \overline{A \wedge \overline{B}} = \text{INV (NAND (A, \overline{B}))} \quad (66)$$

and,

$$\overline{(A \rightarrow (B \rightarrow C))} = \overline{\overline{A \wedge B \wedge \overline{C}}} = \text{INV (NAND (A, B, \overline{C}))} \quad (67)$$

Although the law is stated for two and three inputs only, its applicability can be expanded to accommodate any number of inputs. In each instance, the non-inverted input will consistently appear as its own complement accompanied by the modification in operators as described above.

5) *Principle of Duality*: Traditionally, the 'dual' of a Boolean function is derived by replacing the ANDs (ORs) and 1s (0s) with ORs (ANDs) and 0s (1s), respectively. For instance, the dual of $(A \vee B)$ is $(A \wedge B)$, and $(D \vee 1)$ is the dual of $(D \wedge 0)$.

Theorem 13: Boolean duals for expressions involving asymmetric logic can be found by following the below steps in order:

- Replace all ANDs with ORs, and vice versa.
- Replace all 1s with 0s, and vice versa.
- Change all IANDs to ORs with all inverted inputs complemented.
- Replace all IMPLY with ANDs and complement all of the inverted inputs.

For example, the dual of the Boolean expression $(A \wedge B) \wedge C$ is $(A \vee \overline{B} \vee \overline{C})$, and that of $A \rightarrow (B \rightarrow C)$ becomes $(\overline{A} \vee \overline{B} \vee C)$.

C. Canonical Normal Forms for Asymmetric Logic

Boolean Algebra defines two types of canonical normal forms: the canonical disjunctive normal form (CDNF) and the canonical conjunctive normal form (CCNF). The IAND/OR and IMPLY/NAND are fundamental logic sets capable of representing any Boolean function. Hence, it is vital to define the canonical normal forms for these logic sets.

1) *Canonical Disjunctive Normal Form (CDNF)*: CDNF, commonly referred to as the minterm canonical form or canonical sum of products (SOP), is a Boolean expression derived through the logical 'OR-ing' (disjunction) of specific 'AND-ed' (conjunction) Boolean literals. (68) presents an example.

$$f_{sop}(A, B, C) = (A \wedge B \wedge C) \vee (A \wedge \overline{B} \wedge \overline{C}) \quad (68)$$

In the context of the IAND/OR logic set, the CDNF is proposed as the Sum of IANDs (SOI), characterized by the logical OR operation applied to specific Boolean literals that are combined through the IAND operation in various configurations. For instance,

$$f_{soi}(A, B, C) = ((A \wedge B) \wedge C) \vee ((A \wedge \overline{B}) \wedge \overline{C}). \quad (69)$$

For the IMPLY/NAND logic set, the CDNF is proposed as canonical NAND of implication (NOI), which is the NAND of Boolean literals IMPLY-ed in different combinations. For example,

$$f_{noi}(A, B, C) = \overline{(\overline{A} \rightarrow (B \rightarrow C)) \wedge (A \rightarrow (B \rightarrow C))}. \quad (70)$$

2) *Canonical conjunctive normal form (CCNF)*: CCNF is essentially the dual of CDNF and is also known as a maxterm or product of sums (POS). For example,

$$f_{pos}(A, B, C) = (A \vee B \vee C) \wedge (A \vee \bar{B} \vee C) \quad (71)$$

CCNF for the IAND/OR and IMPLY/NAND logic sets is proposed as IAND of sums (IOS) and IMPLY of NANDs (ION) respectively. Examples for each of these are presented below:

$$f_{ios}(A, B, C) = (A \vee B \vee C) \wedge (\bar{A} \vee B \vee C) \quad (72)$$

$$f_{ion}(A, B, C) = (\bar{A} \wedge B \wedge C) \rightarrow (\bar{A} \wedge B \wedge C) \quad (73)$$

D. Relationship between IAND and Implication Logic (De Morgan Duality)

Further analysis of the De Morgan's law for asymmetric logic function reveals an interesting relationship between IAND and IMPLY operations. Per (59):

$$\overline{(A \rightarrow B)} = A \wedge \bar{B} \quad (74)$$

The RHS of the above equation can be expressed as an IAND of A and B ,

$$\overline{(A \rightarrow B)} = A \wedge B \quad (75)$$

Refactoring LHS of (75) as per Theorem 1,

$$\overline{(A \rightarrow B)} = \bar{B} \wedge \bar{A} \quad (76)$$

For three literals, it can be demonstrated that

$$\overline{(A \rightarrow (B \rightarrow C))} = (\bar{C} \wedge \bar{B}) \wedge \bar{A}. \quad (77)$$

The converse of (74) and (77) are also true,

$$\overline{(A \wedge B)} = \bar{B} \rightarrow \bar{A}, \quad (78)$$

and,

$$\overline{((A \wedge B) \wedge C)} = \bar{C} \rightarrow (\bar{B} \rightarrow \bar{A}). \quad (79)$$

The De Morgan dual for any conventional logic operation can be calculated as

$$f_d(a_1, a_2, a_3 \dots a_n) = \overline{f(\bar{a}_1, \bar{a}_2, \bar{a}_3 \dots \bar{a}_n)}. \quad (80)$$

Remarkably, observations from (74)-(79) reveal the general expression for evaluating the De Morgan dual for any IAND/IMPLY Boolean function:

$$f_d(a_1, a_2, a_3 \dots a_n) = \overline{f(\bar{a}_n, \bar{a}_{n-1}, \bar{a}_{n-2} \dots \bar{a}_2, \bar{a}_1)} \quad (81)$$

where f_d and f are IAND and IMPLY functions respectively (or vice versa). As noted earlier in the paper, the order of operation must be maintained when applying the above relationship. Considering the concepts and observations presented in this section along with section (III-B4), it can be asserted that IAND and IMPLY operations are "De Morgan duals" of each other. This relationship also facilitates the conversion of an SOI expression to its equivalent NOI (or vice versa).

IV. CONCLUSION

In this paper, we presented a comprehensive set of algebraic identities and theorems customized for asymmetric logic func-

tions, particularly focusing on the logic sets fundamental to the bilayer avalanche spin-diode and memristor. This algebra marks a significant step towards optimizing computation for emerging technologies reliant on such functions by providing a foundational framework for optimizing logic circuits without conversion to and from conventional Boolean algebra. By leveraging the unique properties of non-commutative IAND and IMPLY operations, we have shown significant computational advantages, exemplified by the 28% reduction in computational step count for a memristive full adder circuit. It is clear that embracing the inherent asymmetry of certain logic functions and developing specialized algebraic tools that harness their potential can pave the way for more efficient and advanced logic design paradigms in the era of post-CMOS computing.

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