

Optimized Soft-Aided Decoding of OFEC and Staircase Codes

Lukas Rapp⁽¹⁾, Sisi Miao⁽²⁾, Laurent Schmalen⁽²⁾

⁽¹⁾ *now with* Research Laboratory of Electronics (RLE), MIT, Cambridge, MA 02139 USA, rappl@mit.edu

⁽²⁾ Communications Engineering Lab (CEL), Karlsruhe Institute of Technology, Karlsruhe, Germany

Abstract We propose a novel soft-aided hard-decision decoding algorithm for general product-like codes. It achieves error correcting performance similar to that of a soft-decision turbo decoder for staircase and OFEC codes, while maintaining a low complexity. ©2024 The Author(s)

Introduction

Next-generation high-throughput optical communication systems require novel high-performance low-complexity FEC schemes. Product codes (PCs) [1] and its generalizations, e.g., the zipper code family [2] and the OFEC code [3], are suitable candidates. However, traditional soft decision decoding (SDD) based on turbo product decoding (TPD) [4] entails high computational complexity and a high internal decoder data flow. Therefore, even with the existing optimization and simplification methods, e.g., [5],[6], TPD may not meet the energy efficiency requirements for future optical communication systems. This motivates the research on soft-aided hard-decision decoding algorithms, which use hard-message passing as in hard decision decoding (HDD), but introduce a small amount of soft-information to aid the decoder. Our recent soft-aided decoder based on dynamic reliability scores (DRSs) [7],[8] achieves a decoding performance close to TPD for PCs. The DRS is a reliability measurement of the bits which can be updated with hard-messages. The decoding performance improvement stems from approaching miscorrection-free error-and-erasure (EaE) decoding. In this paper, we extend the DRS decoder (DRSD) for general product-like codes. We demonstrate the performance of the decoder on a staircase code [9] and OFEC code [3] with numerical simulations. Significant performance improvements compared to HDD are observed.

GPCs and Channel Model

Generalized PCs (GPCs) are extensions of a PC where every bit is protected by $d_v \geq 2$ component codes \mathcal{C}_c equipped with a component code decoder D_c . For presentation, we consider all component codes \mathcal{C}_c being the same $[n_c, k_c]$ Bose–Chaudhuri–Hocquenghem (BCH) code. For $d_v = 2$, exemplary codes are PCs, staircase codes, zipper codes, and the OFEC code. Codes with $d_v > 2$ are investigated recently in e.g., [10]–[12]. To decode GPCs, an iterative process is executed where a set of component codes are decoded by D_c at a time using a specific schedule until all the words yield a zero syndrome or the maximum num-

ber of decoding iterations is reached. The decoding complexity of GPCs depends on D_c , which is a simple bounded distance decoding (BDD) in HDD, resulting in the ubiquitous iterative BDD (iBDD). In TPD, D_c is a soft-decision decoder with numerous BDD steps followed by soft-message passing.

For binary input additive white Gaussian noise (BI-AWGN) channels with $\sigma_n^2 = (2E_s/N_0)^{-1}$ and BPSK modulation, the probability density function (PDF) of the received absolute value $r \geq 0$ is

$$f_{|R|}(r) = f_R(r | X = +1) + f_R(r | X = -1),$$

with $f_R(r | X = \pm 1)$ being the PDF of $\mathcal{N}(\pm 1, \sigma_n^2)$. The corresponding cumulative distribution function is denoted as $F_{|R|}(r)$.

Proposed Decoder

An overview of the proposed DRSD for GPCs is depicted in Fig. 1. At the initialization step, every bit in the received block is assigned a ternary decision in $\{\pm 1, ?\}$ and a reliability indicator DRS in $\{i_s, i_s + 1, \dots, i_e\}$. A bit is classified as an erasure if its magnitude of the channel output is smaller than the threshold T . In parallel, the DRS values are initialized by a non-uniform quantizer with thresholds $t_{i_s} = 0$ and $\{t_{i_s+1}, \dots, t_{i_e}\}$. A bit with received absolute value $r \geq 0$ is assigned the DRS value $d \in \{i_s, \dots, i_e - 1\}$ if $t_d \leq r < t_{d+1}$ and i_e if $t_{i_e} \leq r$. Here, T and $\{t_{i_s+1}, t_{i_s+2}, \dots, t_{i_e}\}$ are optimizable thresholds. During iterative decoding, the component code decoder D_c decodes every word $\mathbf{y} \in \{0, 1, ?\}^{n_c}$ with an EaE decoder (EaED) followed by a miscorrection detection (MD) step.

We first describe the EaED. Consider a word \mathbf{y} containing E erasures. If $E = 0$, usual BDD is performed. If $\mathbf{y} \in \mathcal{C}_c$, the DRS of every bit in \mathbf{y} is increased by one. If $E > 0$, the erasures are filled with J pairs of distinct random complementary filling patterns, resulting in at most 2^J test patterns. Here, $J = 1$ if $E = 1$ and $J = \min\{\mathcal{J}, E\}$ if $E > 1$, where $\mathcal{J} \in \{1, 2, 3, 4\}$ is configured for a performance-complexity trade-off. Then the test patterns are decoded with BDD, yielding a set \mathcal{I} of unique candidate codewords with $|\mathcal{I}| \leq 2^J$. The duplicated candidate codewords are discarded. If $\mathcal{I} = \emptyset$, a decoding failure is declared and we proceed to decode the next word. If $|\mathcal{I}| > 0$, let

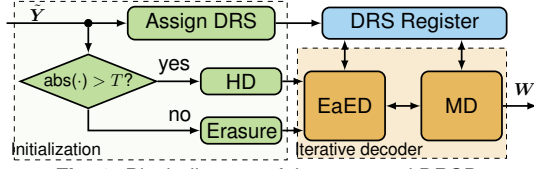


Fig. 1: Block diagram of the proposed DRSD.

$\{c_1, c_2, \dots, c_{|\mathcal{I}|}\} := \mathcal{I}$ such that the Hamming distance between c_{i_1} and \mathbf{y} is smaller than the distance between c_{i_2} and \mathbf{y} at the non-erased position of \mathbf{y} if $i_1 < i_2$.

Then, we perform the MD step for $c_i \in \mathcal{I}$ using a configurable anchor threshold T_a determined based on the code structure. We start with $i = 1$. The bits that have a DRS $> T_a$ are classified as anchor bits and are not allowed to be flipped by D_c . If such anchor bit flips occur, we proceed to the MD step of the next codeword with $i := i + 1$. When no such anchor bit flips occur, the output is $D_c(\mathbf{y}) = c_i$, and the remaining candidate codewords are discarded. In the last step of D_c , the DRS of all flipped bits in c_i is reduced by one. If all $c_i \in \mathcal{I}$ are classified as miscorrections, we reduce the DRS of all flipped bits in c_1 by one. The DRSs are clipped to $[i_s, i_e]$.

DRSD for Staircase Code

We evaluate the decoder for an example staircase code based on a $[255, 231]$ triple-error-correcting BCH code with 1-bit shortening. A sliding-window decoder as in [9] is used with a sliding window of length 7 and 8 decoding iterations. We set $\mathcal{J} = 1$ to use a conventional EaED. For a BI-AWGN channel, we let $i_s = 0$, $i_e = 31$ and calculate the thresholds $\{t_{i_s}, t_{i_s+1}, \dots, t_{i_e}\}$ so that each DRS value is assigned to the same number of bits:

$$t_k = \max \left\{ 0, F_{|R|}^{-1} \left(\frac{(k - i_s)}{(i_e - i_s + 1)} \right) \right\}, \quad (1)$$

where $F_{|R|}^{-1}(\cdot)$ is the inverse function of $F_{|R|}(r)$ and $t_{i_s} = 0$. Let $x \in \{0, 1, \dots, 6\}$ be the distance between the current block being decoded and the end of the current decoding window. We set $T_a = 2(x + 1)$ for $x < 6$ and $T_a = 28$ if $x = 6$. Fig. 2 shows that DRSD outperforms the other soft-aided decoders and yields a significant decoding performance gain compared to iBDD.

DRSD for OFEC code

The OFEC code is a spatially-coupled GPC based on the $[256, 239, t = 2]$ singly extended BCH code where the code extension allows decoding of one additional erasure. As depicted in Fig. 3, which is based on Fig. 20 in [3], the code consists of square blocks of 16×16 bits organized in a matrix of square block rows and columns. Each component code is split in half (front and back). The back protects a row in a square block row and the front protects multiple columns in diagonally arranged square blocks that were earlier encoded. Each bit in the structure is part of the front and back of two

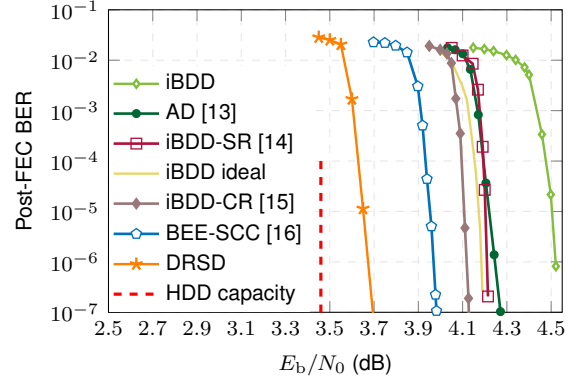


Fig. 2: BER results of a rate 0.811 staircase codes with 1-bit shortened $[255, 231]$, $t = 3$ BCH code as component code.

codewords. We propose the following modifications to the decoder to ensure compatibility with the structure of the OFEC code.

DRS Initialization: We consider a variation of (1) that only quantizes reliabilities below a threshold $t_{\text{quan}, \max} \in \mathbb{R}_{\geq 0}$:

$$t_k = \max \left\{ 0, F_{|R|}^{-1} \left(\frac{k - i_s}{i_e - i_s} F_{|R|}(t_{\text{quan}, \max}) \right) \right\}. \quad (2)$$

Bits with received magnitude $|r| > t_{\text{quan}, \max}$ are assigned the maximal DRS value i_e . This adjustment is made to accommodate some practical implementations, where a maximum quantization value exists for a quantizer.

Tracking Decoding Iterations: For the OFEC code, the anchor threshold is determined as

$$T_a = \begin{cases} T_{a, \text{step}} \left\lfloor \frac{\ell - 1}{p_a} \right\rfloor + T_{a, \text{init}}, & \text{for } \ell \leq 2L - p_r, \\ T_a^*, & \text{for } \ell > 2L - p_r. \end{cases} \quad (3)$$

where $T_{a, \text{init}}$ is the initial anchor threshold and p_a , p_r and $T_{a, \text{step}}$ are new parameters to control T_a . Therefore, it is essential to know the current decoding iteration $\ell \in \mathbb{N}$. However, in the OFEC code, new blocks of bits are added in each decoding iteration and there is no single iteration ℓ . A way to address this issue is to store the number of decoding iterations ℓ_i that have been applied to each bit y_i and calculate T_a individually for each bit using (3), which requires additional storage. This is used in our simulations. Alternatively, we derive from the OFEC structure that ℓ_i can be calculated as $\ell_i = 2 \lfloor \tilde{R}_i / 20 \rfloor + \mathbb{1}_{\{a\}} + \mathbb{1}_{\{b\}}$ where condition $a := \lfloor (\tilde{R}_i \% 20 - 6) / 2 \rfloor \geq 7 - C_i$ and condition $b := \{ \tilde{R}_i \text{ is the first or the second first buffer row} \}$. Here, R_i and C_i denote the square block row and column index of the bit, respectively, and $\tilde{R} = R - R_{\text{current}}$ denotes the relative index with respect to the most recently added row R_{current} . This eliminates the need for additional storage.

Stall Pattern Removal (SPR): Due to the hard-decision nature of the DRSD, a higher error floor than for TPD is expected. As DRSD effectively avoids miscorrections during iterative decoding,

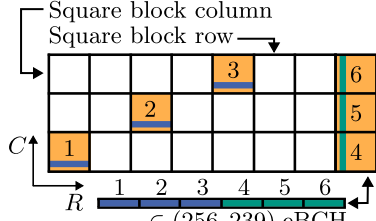


Fig. 3: OFEC Code with 3 instead of 8 square block columns for clarity. Blue and green stripes represent the front and back of the component code, respectively.

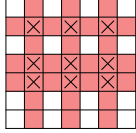


Fig. 4: MSP of a product code with $(t = 2)$ -error correcting component codes.

minimal stall patterns (MSPs) are dominant at the error floor region. Figure 4 depicts a MSP in a PC block. In the PC, decoding a codeword with 3 errors results in a decoding failure or a miscorrection. If these errors are arranged in a 3×3 grid, iterative decoding will fail. As the OFEC code is spatially coupled, errors due to MSPs are distributed over several square block rows. However, because every bit is protected by two codewords, they can be understood similarly to MSPs in a simple PC block. MSPs of the OFEC code can be detected and removed via bit flips [17]:

- (1) Two flags are assigned to each bit to indicate whether its last decoding in the front or back of a codeword failed, respectively.
- (2) After $L - 1$ full decoding iterations of a square block row, its bits with both flags being positive are flipped, followed by 1 decoding iteration to clean up the remaining errors.

Hyperparameter Optimization: DRSD depends on several parameters ($i_s, i_e, T, T_{a,init}, T_{a,step}, T_a^*, p_a$ and p_r) that are optimized for the OFEC code with the hyperparameter optimization tool Optuna [18]: Optuna iteratively samples the best hyperparameters based on previous simulation results. The objective function is the SNR threshold at which the simulated BER is 10^{-4} . The threshold is simulated using the methods described in [19]. In a second optimization round, the parameters are fine-tuned using the BER at a fixed SNR as the objective function.

Simulation Results

We consider the following transmission model: The OFEC encoder (i.e., *ENC0* in Fig. 19 in [3]) encodes blocks of 3552 uniformly distributed information bits into 4096 code bits, which are mapped to QPSK symbols using a Gray code [3] and transmitted over an AWGN channel. We model this as the transmission of two independent BPSK symbols with an amplitude $\frac{1}{\sqrt{2}}$ affected by (real-valued)

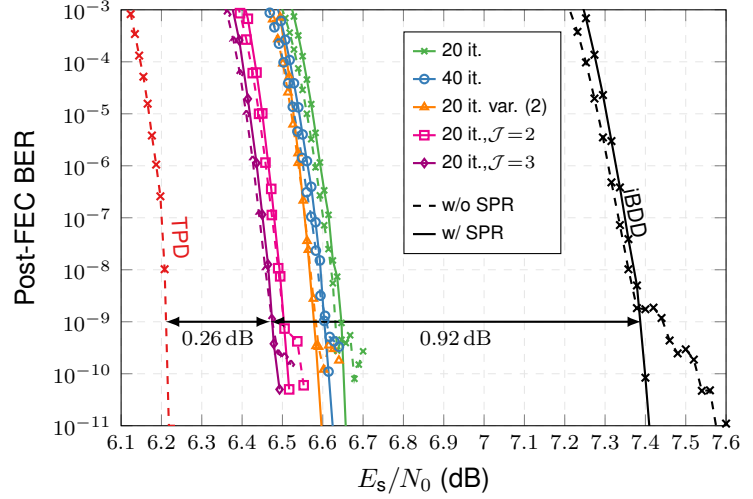


Fig. 5: BER result of the proposed soft-aided DRSD and its variations.

AWGN noise $\sigma_n^2 = (2E_s/N_0)^{-1}$.

We evaluate the decoder by simulating the continuous transmission of OFEC codewords until 10^{12} bits are transmitted or 10^6 bit errors occur. We compare DRSD with iBDD and the OFEC soft decision decoder (TPD). TPD decodes each OFEC square block row with three soft-decision decoding iterations followed by two hard-decision decoding iterations (Appendix III in [20]), where the Chase decoder uses 42 test patterns.

For $J = 1$, DRSD with 20 and 40 full decoding iterations outperforms iBDD at a BER of 10^{-9} by around 0.74 dB and 0.78 dB, respectively. These results use the DRS quantization method (1). Using variation (2) with $t_{quan,max} = 0.9$ while keeping the other optimized parameters improves the performance further (labeled as *20 it. var. (2)*). Increasing J to 2 and 3 leads to a decoding gain of 0.89 and 0.92 dB compared to iBDD, respectively. Further increasing of the J value does not improve the performance significantly.

An error floor below a BER of 10^{-9} is observed when no SPR is used (dashed curves). However, all error floors can be removed with the aforementioned bit flipping SPR (solid curves), i.e., no bit error occurred when simulating up to 10^{12} bits.

DRSD requires more storage and involves ternary message passing compared to the HDD iBDD decoder. However, the level of message passing remains significantly lower than that of TPD. The additional BDD steps caused by erasures, as compared to iBDD, are negligible since erasures are resolved after initial iterations, simplifying EaED to BDD.

Conclusion

We propose a generalized low-complexity hybrid decoding scheme for PC-like codes. Numerical simulation results for two example codes demonstrate performance improvements compared to traditional HDD.

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