

# FPGA Digital Dice using Pseudo Random Number Generator

A PREPRINT

Michael Lim Kee Hian, Ten Wei Lin, Zachary Wu Xuan, Stephanie-Ann Loy, Maoyang Xiang, T. Hui Teo\*

Engineering Product Development

Singapore University of Technology and Design

\*Corresponding Author: [tthui@sutd.edu.sg](mailto:tthui@sutd.edu.sg)

*These authors contributed equally to this work.*

## ABSTRACT

The goal of this project is to design a digital dice that displays dice numbers in real-time. The number is generated by a pseudo-random number generator (PRNG) using XORshift algorithm that is implemented in Verilog HDL on an FPGA. The digital dice is equipped with tilt sensor, display, power management circuit, and rechargeable battery hosted in a 3D printed dice casing. By shaking the digital dice, the tilt sensor signal produces a seed for the PRNG. This digital dice demonstrates a set of possible random numbers of 2, 4, 6, 8, 10, 12, 20, 100 that simulate the number of dice sides. The kit is named SUTDicey.

Keywords: digital dice, pseudo random number generator, FPGA, hardware description language.

## I. Introduction and Implementation

SUTDicey is a hardware module (Figure 1) that provides an interactive solution for simulating dice rolls, offering users the ability to select and roll various types of dice, from 2-sided to 100-sided. Integrated with a tilt sensor and pseudorandom number generator (PRNG), it enables the real-time display of dice roll results on a 7-segment display, delivering an engaging experience for gaming and other applications.

The BOM is summarized in Table 1 for reference. Each Verilog HDL module's behaviour is also given for those who are interested in making similar digital dice.

### RNG Computation

The XORshift algorithm used was adapted in this design, as this algorithm has the significant advantage of speed for real-time application, [1,2]. An XORshift algorithm works by taking the exclusive or (XOR) of a number with a shifted version of itself multiple times, before feeding back into the input again.

The use of a 32-bit seed in the XORshift method makes the randomness seemingly close to a true random number generator (TRPG). A UART connection was used to plot a statistical distribution and evaluate the randomness of the generated XORshift outputs.

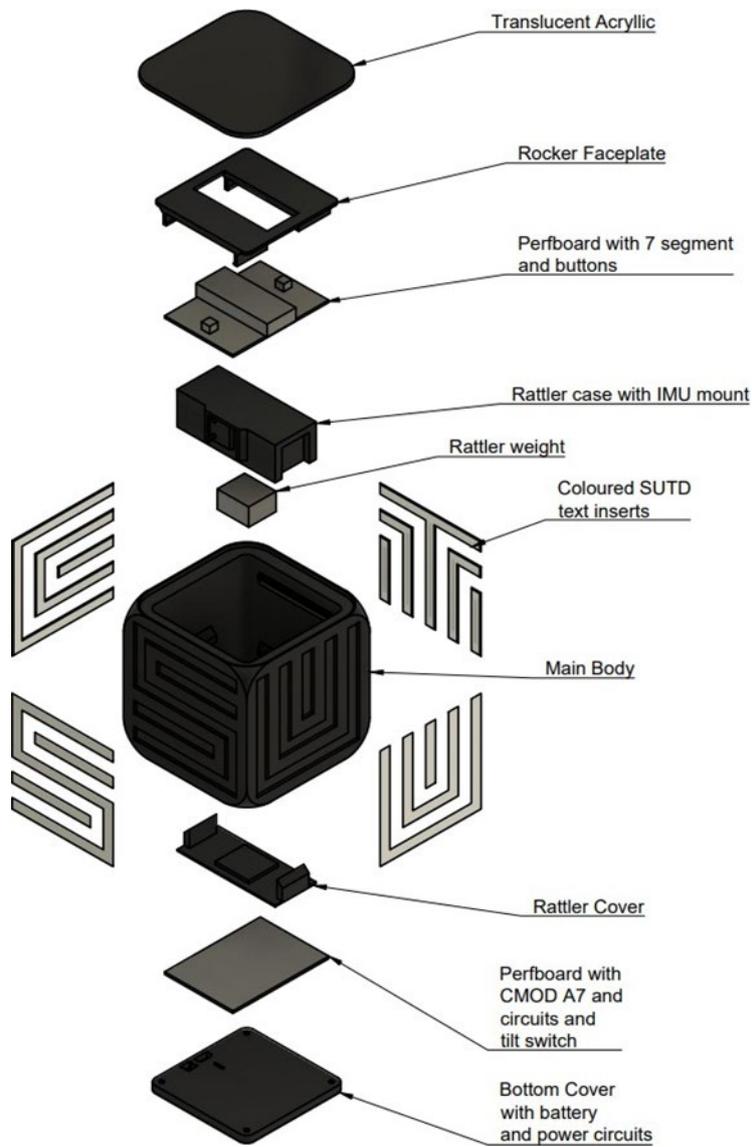


Figure 1: Exploded view of SUTDicey.

Table 1: Bill Of Materials

CMOD A7 35T	Accelerometer adxl335
Tilt Switch sw-520d	Steel Weight for rattler
3D printed parts (see Figure 1)	3x 9.1k ohm resistors
USB-C PD trigger (5v)	3x 10k ohm resistors
Dc-Dc battery charge/discharge module (5v)	3x 6mm tactile pushbutton
3.3v dc-dc step down synchronous buck regulator D24V10F3	3.7v LiPo battery
7 segment display 5643BH	Translucent Acrylic Faceplate
4x 3Mx4 heat-set threaded inserts	4x 3Mx8 hex head screws
2x perforated board 70mmx50mm	

Various electronics components such as CMOD-A7, battery, DC-DC Charge Discharge Integrated Module, Step-down voltage regulators, power push button, up/down push button, tilt switch and resistors (9.1k & 10k) were used and interconnected based on Figure 2.

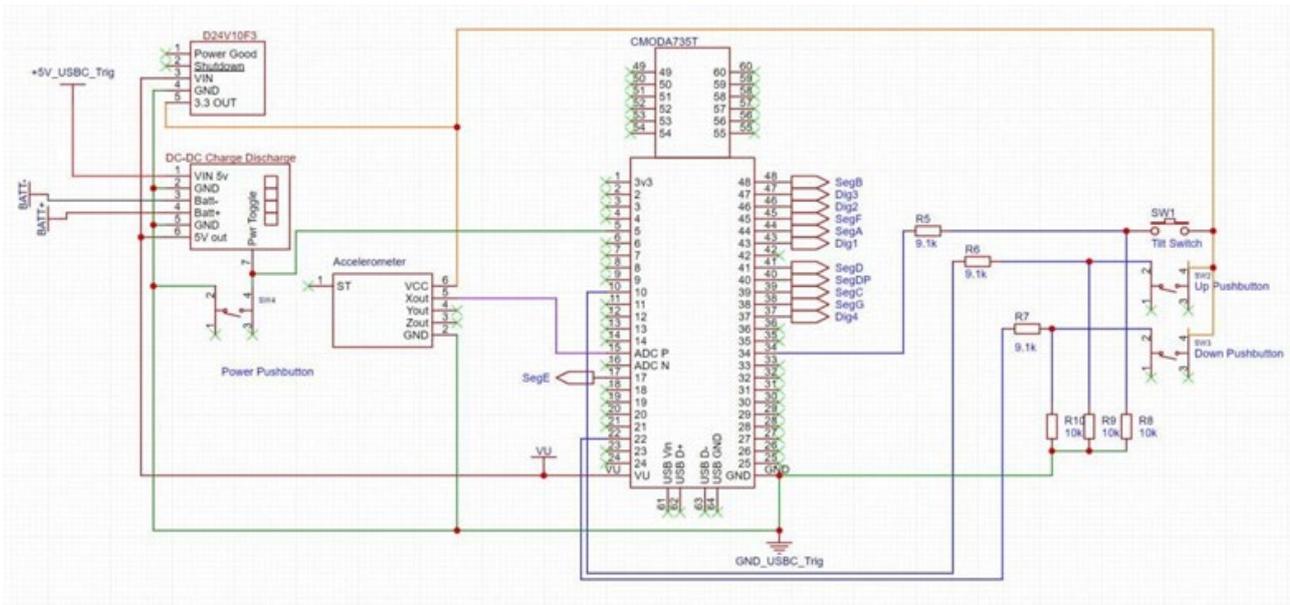


Figure 2: Wiring Circuit for SUTDicey.

## Constraint File

The constraint file is intended for the CmodA7 rev. B FPGA board. It defines pin assignments and I/O standards for various peripherals and interfaces.

To implement the file in the project simply:

1. Uncomment lines corresponding to used pins
2. Rename the ports (in each line, after get\_ports) according to the top-level signal names in the project.

Furthermore, it's worth noting that the file also contains a commented-out line. If uncommented, it permits combinational logic loops with a warning severity level.

## Top Module

This section summarises the functionality and behavioural description of each block in the top module Verilog file.

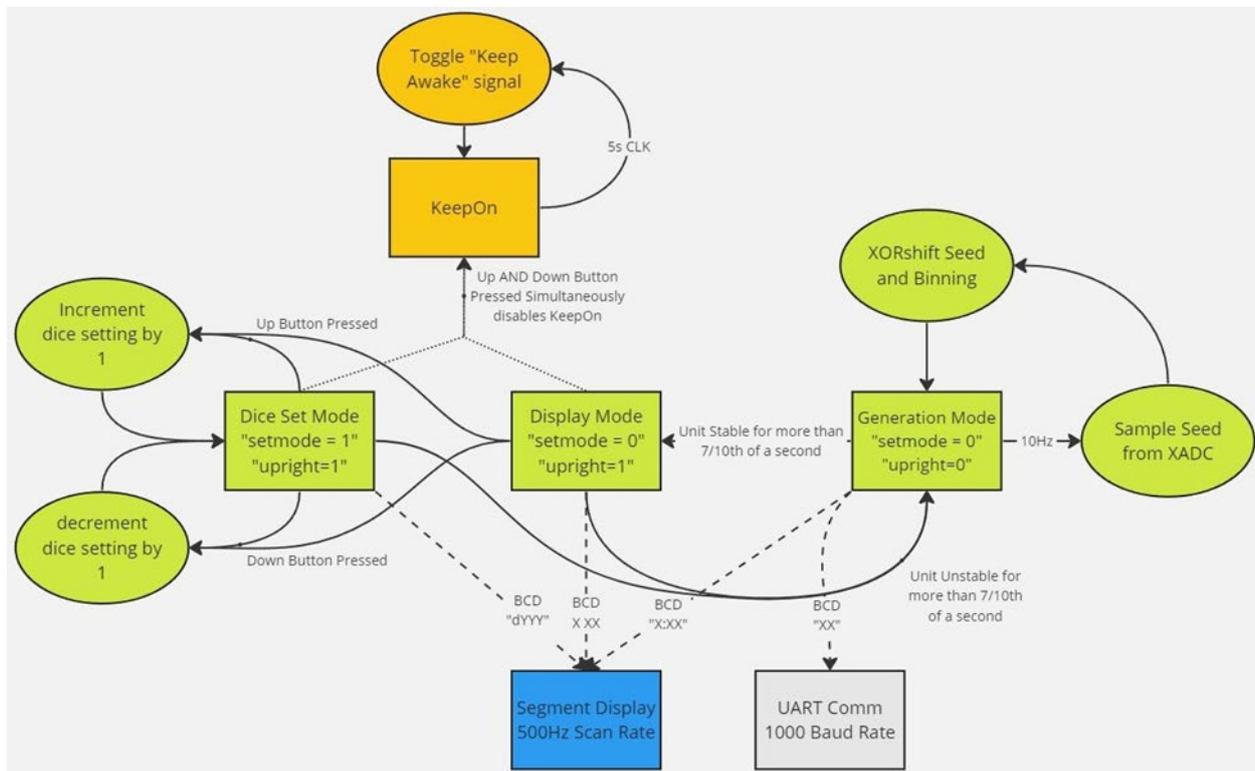


Figure 3: Simplified State Flow Chart (Solid lines represent state changes, broken/dotted lines represent information flow Colours represent separate loops).

## Tilt Detection

Continuously monitors the state of a tilt sensor to determine whether a dice unit is upright and stable.

Behavioural Description:

1. Initialization and Reset Handling:
  - Upon system initialization or a reset signal (rstn), the system resets its internal state.
  - sumtilt is reset to 0, indicating no prior detection of the tilt sensor being in an "on" state.
  - The tiltlog shift register is cleared, ensuring a fresh start for storing tilt sensor readings.
  - The upright flag is set to 0, indicating that the dice unit is not currently detected as upright.
2. Continuous Monitoring and Upright Determination:
  - The system continuously monitors the state of the tilt sensor by sampling it at each positive edge of the CLK10Hz signal.
  - The current state of the tilt sensor is stored in the tiltlog shift register, replacing the oldest recorded state.
  - The sum of the bits in the tiltlog register is calculated, representing the duration the tilt sensor has been in the "on" state over a specific period (approximately 1 second).
  - If the sum of the tiltlog register exceeds a predetermined threshold (7), indicating that the tilt sensor has been consistently in the "on" state for a certain duration (about 7/10th of a second), the system sets the upright flag to 1.
  - If the sum of the tiltlog register is below the threshold, the upright flag remains at 0, indicating that the dice unit is not considered upright and stable.

## Dice Selection and Display

This block manages the control flow of the dice controller, allowing users to interact with it to set the dice value (2,4,6,8,10,12,20,100-sided dice) and mode based on button presses.

#### Behavioural Description:

- On a clock edge or reset, it initializes/reset various signals and variables.
- It updates the states of the "up" and "down" buttons (btnUr and btnDr).
- It checks if the dice is upright (upright) and processes button presses accordingly:
  - If both the "up" and "down" buttons are pressed simultaneously, it disables the keep awake feature (keepon).
  - If only the "up" button is pressed, it enters the set mode and cycles through dice values (dselect).
  - If only the "down" button is pressed, it enters the set mode and cycles through dice values in reverse.
- It updates the displayed value on the segment display (thou\_set, hunns\_set, tens\_set, ones\_set) based on the selected mode (dselect).
- If the dice is not upright, it exits the set mode.

## Dice Selection and Display

This block manages the control flow of the dice controller, allowing users to interact with it to set the dice value (2,4,6,8,10,12,20,100 sided dice) and mode based on button presses.

#### Behavioural Description:

- On a clock edge or reset, it initializes/reset various signals and variables.
- It updates the states of the "up" and "down" buttons (btnUr and btnDr).
- It checks if the dice is upright (upright) and processes button presses accordingly:
  - If both the "up" and "down" buttons are pressed simultaneously, it disables the keep awake feature (keepon).
  - If only the "up" button is pressed, it enters the set mode and cycles through dice values (dselect).
  - If only the "down" button is pressed, it enters the set mode and cycles through dice values in reverse.
- It updates the displayed value on the segment display (thou\_set, hunns\_set, tens\_set, ones\_set) based on the selected mode (dselect).
- If the dice is not upright, it exits the set mode.

## XADC Analog Input to 32-bit Seed Generator

This module converts XADC analogue input to a 32-bit seed using a shift register. It accumulates ADC data on each positive clock edge, generating (Segment\_Data) as the seed PRNG.

#### Behavioural Description:

- On the positive edge of the clock signal (CLK10Hz), or upon a negative reset (rstn), the module either resets the seed value to zero or shifts in new ADC data.
- If a reset occurs, the seed value is reset to zero.
- Otherwise, the module shifts the current seed value left by 16 bits and assigns the lower 16 bits to the newly acquired ADC data.
- This results in the generation of a 32-bit value in (Segment\_Data) as a seed for PRNG.

## Segmented Display Processing

Processes the raw RNG values generated by the PRNG algorithm and prepares them for display on a segmented display.

Behavioural Description:

- The raw RNG values (rand) are generated by the pseudo-random number generator (PRNG) algorithm discussed earlier.
- These raw RNG values are fed into the display processing logic to convert them into BCD (Binary Coded Decimal) format for display.
- The RNG values are modulo-ed by a dice value to normalize them into the desired range for the dice game. Essentially involves converting a wide range of RNG values into a smaller range suitable for a dice roll (e.g., converting from a 32-bit range to a 1-6 range for a six-sided dice).
- The processed RNG values are then converted to BCD format for display on the segmented display.

## Segment Display Control

The 7-segment display can be set manually or generated randomly.

Behavioural Description:

- Four variables ones\_bcd, tens\_bcd, huns\_bcd, and thou\_bcd, each 4 bits wide, representing the BCD (Binary Coded Decimal) values for ones, tens, hundreds, and thousands places.
- If setmode is true, it sets the BCD values directly from thou\_set, huns\_set, tens\_set, and ones\_set. If setmode is false, it sets the BCD values based on some random values (thou\_rand, huns\_rand, tens\_rand, ones\_rand), with some conditions.
- BCD values are assigned to bcd\_tim in the appropriate order for display.

## Battery Module

It toggles a pin every 5 seconds to prevent the module from shutting down due to low current draw from FPGA. The keep-awake function can be disabled by pressing both up and down buttons simultaneously.

## UART Interface (Communication)

Controls the rate of message transmission and outputs data representing the tens and ones value of a dice roll through UART

Behavioural Description:

- uart\_ready toggles on each positive clock edge, controlling the message transmission rate.
- Data is sent over UART when uart\_ready is high and uart\_valid is asserted.
- The UART interface operates asynchronously, transmitting data via uart\_rxd\_out.
- The display cycles through the digits at a rate of 500 Hz (clk500hz).

## Segment Module

Controls a 4-digit 7-segment display, sequentially showing each digit of a BCD number.

### Behavioural Description:

- The module sequentially displays each digit of the BCD number on the 7-segment display.
- An internal register (an\_r) determines which digit is currently being displayed, cycling through each digit in sequence.
- The BCD number to be displayed is selected based on the value of an\_r.
- The BCD number is converted into the corresponding 7-segment code and stored in an internal register (segment\_r).
- On reset (rstn), all displays are turned off and overwritten with “dddd”.

## UART TX Module

The UART transmitter module is designed to transmit serial data asynchronously to a receiver. It operates based on a finite state machine (FSM) to control the transmission process. The module handles data transfer, start and stop bit insertion, and optionally, parity bit generation for error detection.

### Behavioural Description:

- The module uses an FSM to manage the transmission process. The FSM transitions between states including IDLE, START, TRANSFER, and STOP based on various conditions such as readiness of the receiver (ap\_ready).
- When data is ready (ap\_ready), the module starts the transmission process by sending a start bit (FSM\_STAR). It then proceeds to transmit each bit of the data (data) followed by an optional parity bit (parity) and a stop bit (FSM\_STOP).
- The module generates output signals (ap\_valid and tx) to indicate the validity of the transmitted data and the actual serial data stream, respectively.
- Synchronous reset (ap\_rstn) is used to initialize the module to the IDLE state.
- Optionally, the module can perform parity checking (FSM\_PARI) to ensure data integrity, although the implementation for this is currently commented out.

## Random Number Generation for Dice Roll

A pseudorandom number generator (PRNG) is used to generate random numbers for the dice rolls. The PRNG algorithm takes seed values obtained from a XADC and produces pseudorandom values, which are used for generating the dice roll results.

### Behavioural Description:

- On each rising edge of the system clock (sysclk), the PRNG computes the next pseudo-random number.
- It uses the previous pseudo-random number (stored in rand\_reg) to compute the next value.
- The computation involves bitwise XOR and shifting operations.
- The result is stored in a register (rand\_reg) synchronously to avoid combinatorial loop issues.
- The pseudo-random number is outputted as rand for further use in the FPGA design.

```
1. reg [31:0] temp;
2. reg [31:0] temp2;
3. reg [31:0] rand;
4.
5. //Pseudo-Random XOR shift register algorithm with seed value supplied by XADC
6. always@(sysclk)begin
7. temp = Segment_data ^ Segment_data >>7;
8. temp2 = temp ^ temp << 9;
9. rand = temp2 ^ temp2 >> 13;
10. end
```

The generated PRNG numbers are plotted in Figure 4, and Figure 5, which show the randomness.

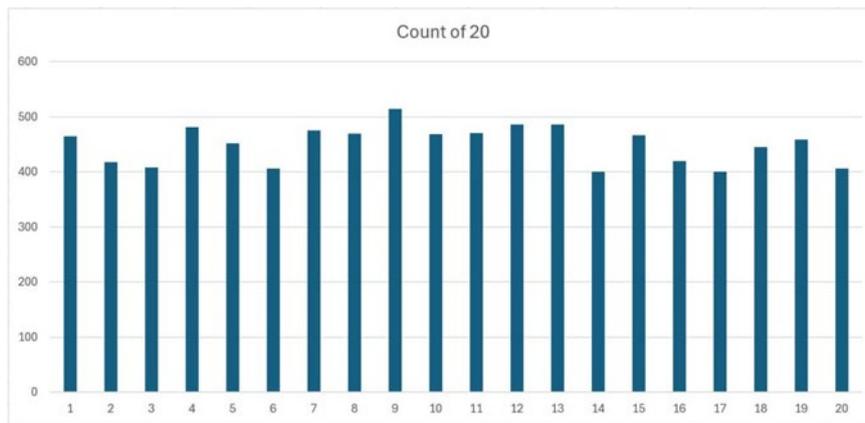


Figure 4: Statistical distribution for 20-sided dice.

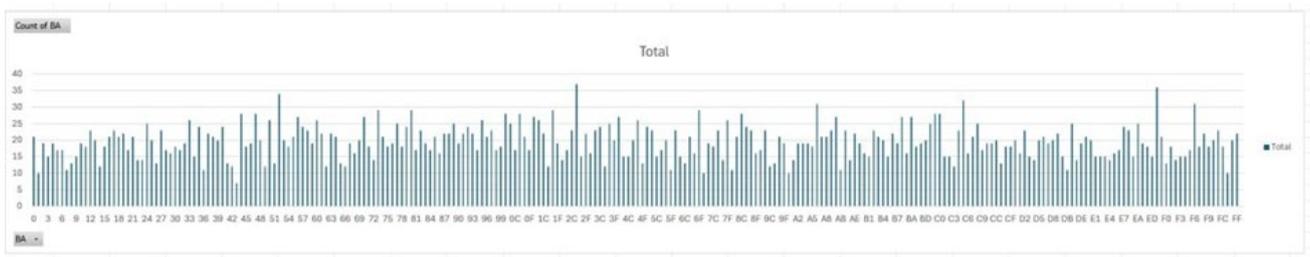


Figure 5: Statistical distribution before RNG value is converted to the chosen dice range.

## II. Operation of SUTDicey

This section is dedicated to user guides for using the dice. The key steps are given below.

1. Power on SUTDicey by pressing the recessed button on the bottom of the unit, a red light should show in the slot nearby.
  - a. If a red light does not show, the unit is probably out of power, please charge it with a USB C cable (5 V mode)
2. Place the SUTDicey unit upright, with the smooth acrylic side facing up, it will take a few seconds to “boot” up. When numerals are displayed through the acrylic face, it has completed booting.
3. Press above or below on the acrylic face to change between the d2, d4, d6, d8, d10, d12, d20 and d100-sided dice.
  - a. Pressing both up and down buttons at the same time while the dice is upright will initiate shutdown which will occur after around 15-30 seconds.
4. To roll the selected dice, tilt upside down or shake the SUTDicey unit for more than one second, a colon in the middle of the display will light to show that the unit is not stable and is “tossing/scrambling” the dice. The display numbers will also scramble and randomize.
5. Place or hold the unit upright for more than a second to “roll” the die. The colon in the middle of the display will disappear once the die is “stable” and has “settled” on a final value. Be careful not to shake or upset the SUTDicey unit as it will roll the dice again if it detects enough movement.
6. Shaking or tilting the SUTDicey unit will roll the last type of dice selected.

## Summary

A complete design of a digital dice using PRNG is demonstrated in the work. More work to be done in improving the implementation of the PRNG algorithm in FPGA is required for better randomness that meeting actual dice's behaviour.

## Acknowledgments

We would like to thank SUTD-ZJU IDEA Visiting Professor Grant (SUTD-ZJU (VP) 202103, and SUTD-ZJU Thematic Research Grant (SUTD-ZJU (TR) 202204), for supporting this work.

## References

- [1] Hammond, J. (2022). FPGA Random Number Generator. arXiv:2209.04423, <https://doi.org/10.48550/arXiv.2209.04423>
- [2] Marsaglia, G. (2003). Xorshift RNGs. Journal of Statistical Software, 8(14), 1–6. <https://doi.org/10.18637/jss.v008.i14>

## Appendix

```
1. module top_module(  
2.     input sysclk,  
3.     input tilt,  
4.     input btnU,  
5.     input btnD,  
6.     input [1:0] btn,  
7.     output onpin,  
8.     output [6:0] seg, // 7-Segment - Segment[6:0];  
9.     output dp,      // 7-Segment - Segment-DP;  
10.    output [3:0] an, // 7-Segment - Common Anode;  
11.    output [1:0] led,  
12.    input vp_in,  
13.    input vn_in,  
14.    input [1:0] xa_n,  
15.    input [1:0] xa_p,  
16.    output uart_rxd_out  
17. );  
18.  
19. reg CLK1000Hz, CLK1500Hz, CLK500Hz, CLK10Hz, CLK5s;  
20. wire [15:0] bcd_tim;  
21. wire rstn;  
22. reg keepon;  
23. reg onsig;  
24. reg clk5;  
25.  
26. assign rstn=~btn[0];  
27. assign led[1]=tilt;  
28. assign led[0]=clk5;  
29.  
30. reg [12:0] CLK_CNTER_1000Hz;  
31. reg [12:0] CLK_CNTER_1500Hz;  
32. reg [13:0] CLK_CNTER_500Hz;  
33. reg [19:0] CLK_CNTER_10Hz;  
34. reg [24:0] CLK_CNTER_5s;  
35.  
36. //Generate 1000Hz CLK;
```

```

37. always@(posedge sysclk, negedge rstn)begin
38.     if(!rstn) begin
39.         CLK_CNTER_1000Hz<=13'd0;
40.         CLK1000Hz <= 1'b0;
41.     end
42.     else begin
43.         if(CLK_CNTER_1000Hz == 13'd6000-1'b1) begin
44.             CLK1000Hz <= ~ CLK1000Hz;
45.             CLK_CNTER_1000Hz <= 13'd0;
46.         end
47.         else CLK_CNTER_1000Hz <= CLK_CNTER_1000Hz + 1'b1;
48.     end
49. end
50.
51. //Generate 1500Hz CLK;
52. always@(posedge sysclk, negedge rstn)begin
53.     if(!rstn) begin
54.         CLK_CNTER_1500Hz<=13'd0;
55.         CLK1500Hz <= 1'b0;
56.     end
57.     else begin
58.         if(CLK_CNTER_1500Hz == 13'd4000-1'b1) begin
59.             CLK1500Hz <= ~ CLK1500Hz;
60.             CLK_CNTER_1500Hz <= 13'd0;
61.         end
62.         else CLK_CNTER_1500Hz <= CLK_CNTER_1500Hz + 1'b1;
63.     end
64. end
65.
66. //Generate 5s CLK;
67. always@(posedge sysclk, negedge rstn)begin
68.     if(!rstn) begin
69.         CLK_CNTER_5s<=25'd0;
70.         CLK5s<= 1'b0;
71.     end
72.     else begin
73.         if(CLK_CNTER_5s == 25'd30001200-1'b1) begin
74.             CLK5s <= ~ CLK5s;
75.             CLK_CNTER_5s <= 25'd0;
76.         end
77.         else CLK_CNTER_5s <= CLK_CNTER_5s + 1'b1;
78.     end
79. end
80.
81. //Generate 500Hz CLK;
82. always@(posedge sysclk, negedge rstn) begin
83.     if(!rstn) begin
84.         CLK_CNTER_500Hz<=14'h0000;
85.         CLK500Hz <= 1'b0;
86.     end
87.     else begin
88.         if(CLK_CNTER_500Hz == 14'd12_000-1'b1) begin
89.             CLK500Hz <= ~ CLK500Hz;
90.             CLK_CNTER_500Hz <= 14'h0000;
91.         end
92.         else CLK_CNTER_500Hz <= CLK_CNTER_500Hz + 1'b1;
93.     end
94. end
95.
96. //Generate 10Hz CLK;
97. always@(posedge sysclk, negedge rstn)begin
98.     if(!rstn) begin
99.         CLK_CNTER_10Hz<=20'd0;
100.        CLK10Hz <= 1'b0;
101.    end
102.    else begin
103.        if(CLK_CNTER_10Hz == 20'd600024-1'b1) begin
104.            CLK10Hz <= ~ CLK10Hz;
105.            CLK_CNTER_10Hz <= 20'd0;
106.        end
107.        else CLK_CNTER_10Hz <= CLK_CNTER_10Hz + 1'b1;
108.    end
109. end
110.

```

```

111. //XADC IP block setup
112. reg [31:0] Segment_data;
113. wire enable; //enable into the xadc to continuously get data out
114. reg [6:0] Address_in = 7'h14; //Adress of register in XADC drp corresponding to data
115. wire ready; //XADC port that declares when data is ready to be taken
116. wire [15:0] ADC_data; //XADC data
117.
118. xadc_wiz_0 xadc_u0
119. (
120.     .daddr_in(Address_in), // Address bus for the dynamic reconfiguration port
121.     .dclk_in(sysclk), // Clock input for the dynamic reconfiguration port
122.     .den_in(enable), // Enable Signal for the dynamic reconfiguration port
123.     .di_in(0), // Input data bus for the dynamic reconfiguration port
124.     .dwe_in(0), // Write Enable for the dynamic reconfiguration port
125.     .vauxp12(xa_p[1]),
126.     .vauxn12(xa_n[1]),
127.     .vauxp4(xa_p[0]),
128.     .vauxn4(xa_n[0]),
129.     .busy_out(), // ADC Busy signal
130.     .channel_out(), // Channel Selection Outputs
131.     .do_out(ADC_data), // Output data bus for dynamic reconfiguration port
132.     .drdy_out(ready), // Data ready signal for the dynamic reconfiguration port
133.     .eoc_out(enable), // End of Conversion Signal
134.     .vp_in(vp_in), // Dedicated Analog Input Pair
135.     .vn_in(vn_in)
136. );
137.
138. //Read XADC analog input value and store into "Segment_Data" via shift register to create 32 bit seed
value
139. always @(posedge CLK10Hz or negedge rstn) begin
140.     if(!rstn)begin
141.         Segment_data<=0;
142.     end
143.     else begin
144.         Segment_data<=Segment_data<<16;
145.         Segment_data[15:0] <= ADC_data;
146.     end
147. end
148.
149. reg [31:0] temp;
150. reg [31:0] temp2;
151. reg [31:0] rand;
152.
153. //Pseudo-Random XOR shift register algorithm with seed value supplied by XADC, it's not perfect as seed
keeps changing every number
154. always@(sysclk)begin
155.     temp = Segment_data ^ Segment_data >>7;
156.     temp2 = temp ^ temp << 9;
157.     rand = temp2 ^ temp2 >> 13;
158. end
159.
160. //setup for tilt detection and dice selection function
161. reg [15:0] out;
162. reg [3:0] ones_set;
163. reg [3:0] tens_set;
164. reg [3:0] huns_set;
165. reg [3:0] thou_set;
166. reg upright;
167. reg setmode;
168. reg [3:0] dselect;
169. reg [9:0] tiltlog;
170. reg [4:0] sumtilt;
171. reg [6:0] diceval;
172. assign dp = upright;
173. reg btnUr,btnDr;
174.
175. //this function polls the tilt sensor every 1/10th of a second and adds it to a 10 bit shift register, it
adds the total value of the register to the "sumtilt" variable, if a critical number of bits are 1 (meaning the
dice unit has been upright and stable
176. //for enough time, sumtilt>7 aka, the dice was upright for 7/10th of the second) then it sets the upright
register to 1, otherwise it sets it to 0.
177. always@(posedge CLK10Hz or negedge rstn)begin
178.     if(!rstn)begin
179.         sumtilt<=5'b00000;

```

```

180.     tiltlog<=9'b00000000;
181.     upright<=0;
182.     end
183.     else
184.     begin
185.         tiltlog <= tiltlog << 1;
186.         tiltlog[0]<=tilt;
187.
sumtilt=tiltlog[9]+tiltlog[8]+tiltlog[7]+tiltlog[6]+tiltlog[5]+tiltlog[4]+tiltlog[3]+tiltlog[2]+tiltlog[1]+tilt
log[0];
188.     if (sumtilt>=7) begin
189.         upright<=1;
190.     end
191.     else begin
192.         upright<=0;
193.     end
194.     end
195. end
196.
197. //This function detects when the set dice value buttons are pressed only when the dice is upright, and
changes the dice's mode into dice set mode (setmode). pressing the buttons in this mode will allow the value of
the dice (diceval) to be
198. //changed between 2,4,6,8,10,12,20,100 sided dice. The keep awake disable is also here, which requires
both up and down buttons to be pressed at the same time.
199. always@(posedge CLK10Hz or negedge rstn)begin
200.     if(!rstn)begin
201.         thou_set<=0;
202.         huns_set<=0;
203.         tens_set<=0;
204.         ones_set<=0;
205.         btnUr<=0;
206.         btnDr<=0;
207.         dselect<=0;
208.         setmode<=0;
209.         diceval<=2;
210.         keepon<=1;
211.     end
212.     else begin
213.
214.         if(btnU)
215.             btnUr<=1;
216.         else
217.             btnUr<=0;
218.         if(btnD)
219.             btnDr<=1;
220.         else
221.             btnDr<=0;
222.
223.         if(upright)begin
224.             if(btnUr)begin
225.                 if(btnDr)begin
226.                     keepon<=0;
227.                 end
228.             else begin
229.                 setmode<=1;
230.                 if(dselect==7)
231.                     dselect<=0;
232.                 else
233.                     dselect<=dselect+1;
234.             end
235.         end
236.         else if(btnDr)begin
237.             setmode<=1;
238.             if(dselect==0)
239.                 dselect<=7;
240.             else
241.                 dselect<=dselect-1;
242.         end
243.
244.         thou_set<=4'hd;
245.         case(dselect)
246.             4'd0:begin
247.                 huns_set<=2;
248.                 tens_set<=4'hf;

```

```

249.         ones_set<=4'hf;
250.         diceval<=2;
251.     end
252.     4'd1:begin
253.         huns_set<=4;
254.         tens_set<=4'hf;
255.         ones_set<=4'hf;
256.         diceval<=4;
257.     end
258.     4'd2:begin
259.         huns_set<=6;
260.         tens_set<=4'hf;
261.         ones_set<=4'hf;
262.         diceval<=6;
263.     end
264.     4'd3:begin
265.         huns_set<=8;
266.         tens_set<=4'hf;
267.         ones_set<=4'hf;
268.         diceval<=8;
269.     end
270.     4'd4:begin
271.         huns_set<=1;
272.         tens_set<=0;
273.         ones_set<=4'hf;
274.         diceval<=10;
275.     end
276.     4'd5:begin
277.         huns_set<=1;
278.         tens_set<=2;
279.         ones_set<=4'hf;
280.         diceval<=12;
281.     end
282.     4'd6:begin
283.         huns_set<=2;
284.         tens_set<=0;
285.         ones_set<=4'hf;
286.         diceval<=20;
287.     end
288.     4'd7:begin
289.         huns_set<=1;
290.         tens_set<=0;
291.         ones_set<=0;
292.         diceval<=100;
293.     end
294. endcase
295.
296.     end
297.     else
298.         setmode<=0;
299.
300. end
301. end
302. // setup for the raw RNG value to be processed
303. reg [3:0] ones_rand;
304. reg [3:0] tens_rand;
305. reg [3:0] huns_rand;
306. reg [3:0] thou_rand;
307. reg [3:0] ones_randr;
308. reg [3:0] tens_randr;
309. reg [3:0] huns_randr;
310. reg [3:0] thou_randr;
311.
312. //The raw RNG value is processed every 10th of a second, the value is modulo ed by the dice value to
normalise the extended 32 bit range to the required dice range (eg, compressed from 0-4,294,967,295 to 1-6 for
a 6 sided dice) the result is then converted to
313. //a BCD value for display, values are shifted by 10 to centralise the values displayed. The continous
updating gives the "scambled" or "rolling" effect that scrolls through the values on the display.
314. always @(posedge CLK10Hz or negedge rstn) begin
315.     if(!rstn)begin
316.         ones_rand=4'h0;
317.         tens_rand=4'h0;
318.         huns_rand=4'h0;
319.         thou_rand=4'h0;

```

```

320.     end
321.     else if(!upright) begin
322.         out=(rand%diceval)+1; //32 bit to dice range conversion
323.         ones_randr=4'hf; //ones segment disabled
324.         tens_randr = out % 10; // Units digit displayed in tens segment
325.         out = out / 10; // divisor fed to next modulo
326.         huns_randr = out % 10; // Tens digit displayed in hundreds segment
327.         out = out / 10; // divisor fed to next modulo
328.         thou_randr = out % 10; // Hundreds digit displayed in thousands segment
329.
330.         thou_rand=thou_randr;
331.         huns_rand=huns_randr;
332.         tens_rand=tens_randr;
333.         ones_rand=ones_randr;
334.     end
335.     else begin
336.         thou_rand=thou_randr; //if dice is upright, the values are held so they can be read
337.         huns_rand=huns_randr;
338.         tens_rand=tens_randr;
339.         ones_rand=ones_randr;
340.     end
341.     end
342. end
343.
344. //The keep awake function is needed as the battery charge/discharge module turns off after 30 seconds if
current less than 50ma is drawn (the FPGA module current draw tends to dip below 50ma at times, thus it can
sporadically shut off.
345. //the button on the charge/discharge module is a on/off button, if the button is pressed in quick
succession, it turns off, but if it's pressed after a long interval, it will refresh the 30 second shutdown
timer.
346. //the button is triggered by a falling edge pulled to ground.
347. //this function prevents shutdown from happening by pulling the pin low every 10 seconds (5 sec clock)
unless the keep awake is switched off by pressing both up and down buttons simultaneously
348. always @ (posedge CLK5s)begin
349. if(!rstn) begin
350.     onsig<=1;
351.     clk5<=0;
352.     end
353. else if(keepon) begin
354.     onsig<=~onsig;
355.     clk5<=~clk5;
356.     end
357. else begin
358.     onsig<=0;
359.     clk5<=0;
360.     end
361. end
362. assign onpin = onsig;
363.
364. // setup to write values into segment display buffer
365. reg [3:0] ones_bcd;
366. reg [3:0] tens_bcd;
367. reg [3:0] huns_bcd;
368. reg [3:0] thou_bcd;
369. // selects values to be displayed from the dice selection mode or RNG mode based on the state it is in
using the value (setmode)
370. always@(sysclk)begin
371. if(setmode)begin
372.     thou_bcd<=thou_set;
373.     huns_bcd<=huns_set;
374.     tens_bcd<=tens_set;
375.     ones_bcd<=ones_set;
376.     end
377. else begin
378.     if(thou_rand==0)
379.     thou_bcd<=4'hf;
380.     else
381.     thou_bcd<=thou_rand;
382.     if(huns_rand==0 && thou_rand==0)
383.     huns_bcd<=4'hf;
384.     else
385.     huns_bcd<=huns_rand;
386.     if(tens_rand==0 && huns_rand==00 && thou_rand ==0)
387.     tens_bcd<=4'hf;

```

```

388. else
389. tens_bcd<=tens_rand;
390. if(ones_rand==0)
391. ones_bcd<=4'hf;
392. else
393. ones_bcd<=ones_rand;
394. end
395. end
396.
397. //writes to registers to transfer to segment display function
398. assign bcd_tim[15:12] = thou_bcd;
399. assign bcd_tim[11:8]  = huns_bcd;
400. assign bcd_tim[7:4]   = tens_bcd;
401. assign bcd_tim[3:0]   = ones_bcd;
402.
403. //segment display function
404. Segment segment_u0(rstn,CLK500Hz,bcd_tim,{an[0],an[1],an[2],an[3]},seg[6:0]);
405.
406. //uart setup
407. reg uart_ready;
408. wire uart_vaid;
409.
410. //uart control function, this determines the rate at which messages are sent, not to be confused by
bitrate.
411. //has some issues sending messages at a rate lower than 100Hz even though the actual data rate capable by
this system is 100Hz
412. always@(posedge CLK1000Hz,negege rstn)begin
413.     if (!rstn)begin
414.         uart_ready <= 1'b0;
415.     end
416.     else begin
417.         uart_ready <= ~uart_ready;
418.     end
419. end
420.
421. //outputs the value of the 100s and 10s segments (aka the tens and ones value of the diceroll) through
UART for logging in the computer
422. //the signal is passed through the uart_rxd_out pin which is tied to the FT2232HQ USB-UART bridge to
enable communication with the computer rather than needing to have a separate device to act as the middleman.
423. uart_tx uart_tx_u0(CLK1000Hz,rstn,uart_ready,uart_vaid,uart_rxd_out,1'b0,{huns_rand,tens_rand});
424.
425. endmodule

```